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EXAMINER	
ZHE, MENG YAO	

ART UNIT	PAPER NUMBER
2195	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/808,110	YU, YUAN	
	Examiner	Art Unit	
	MENGYAO ZHE	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-19,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-19, 21-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4, 6-19, 21-22 are presented for examination.

Claim Objections

2. Claim 21 objected to because of the following informalities: claim 21 depends on claim 20 that has been cancelled. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 16, 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. The following claim languages are unclear and indefinite:

1) Claim 16, lines 4-5, it is uncertain what "shared memory objects instrumentation information" is <i.e. what is this? What does it do?>

Claim 19 has the same deficiencies as claim 16 above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 6-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tudor, Patent No. 6,920634 (hereafter Tudor) in view of A Comparative Analysis of Fine-Grain Threads Packages, Lowenthal et al., 2001 (hereafter Lowenthal).

7. Tudor was cited in the previous office action.

8. As per claims 1, 4, Tudor teaches a computer-implemented method for dynamically detecting a potential race condition in a program having a plurality of threads and one or more shared memory locations (Column 1, line 67; Column 2 , lines 1-2), the method comprising:

with respect to each shared memory location, maintaining a first set of locks associated with the location, and maintaining a set of concurrent thread segments that access said each shared memory location (Column 2, lines 1-7; Column 8, lines 35-43);

with respect to each thread, maintaining a second set of locks that are acquired and released by a thread (Column 2, line 12; Column 8, lines 36-43), and maintaining a set of thread segments that are ordered before a current thread segment of the thread (Fig 6; Column 2, lines 61-65; Column 5, lines 63-67; Column 6, lines 22-33).

Tudor does not specifically teach maintaining a virtual clock associated with each thread, wherein the ordering of the set of concurrent thread segments rely on the virtual clock.

However, Lowenthal teaches maintaining a virtual clock associated with each thread, wherein the ordering of the set of concurrent thread segments rely on the virtual clock (Section 2 General Thread Model, subsection Creation) for the purpose creating threads.

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to modify the teachings of Tudor with maintaining a virtual clock associated with each thread, wherein the ordering of the set of concurrent thread segments rely on the virtual clock, as taught by Lowenthal, because it allows for thread creation.

9. As per claims 6, 7, Tudor does not specifically teach wherein maintaining the virtual clock comprises initializing the virtual clock to zero when the thread is created.

However, it would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to initialize the timer to any amount, including zero, in order to calculate the amount of waiting time.

10. As per claims 2, 3, 8, 11, Tudor teaches maintaining the set of thread segments that are ordered before the current thread segment of the thread in order to track the execution order of threads (Column 2, lines 61-65; Column 5, lines 63-67; Column 6, lines 22-33).

Tudor does not specifically teach maintaining a set of ordered pairs, wherein one member of a pair is a thread identifier, and the other member of the pair is a virtual clock value.

However, it would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to modify the teachings of Tudor with maintaining a set of ordered pairs, wherein one member of a pair is a thread identifier, and the other member of the pair is a virtual clock value since it allows for tracking execution order of threads.

11. As per claims 9, 12, 13, Tudor does not specifically teach if a first thread forks a second thread: computing the set of thread segments that are ordered before the current thread segment of the second thread as the union of (a) the set of thread segments that are ordered before the current thread segment of the first thread and (b) a singleton set containing the current thread segment of the first thread; incrementing the virtual clock associated with the first thread, and initializing the virtual clock associated with the second thread.

However, it would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to modify the teachings of Tudor with if a first thread forks a second thread: computing the set of thread segments that are ordered before the current thread segment of the second thread as the union of (a) the set of thread segments that are ordered before the current thread segment of the first thread and (b) a singleton set containing the current thread segment of the first thread; incrementing the virtual clock associated with the first thread, and initializing the virtual clock associated with the second thread since this is analogous to asking the question of if mother A has her parents and grandparents born before her, and if mother A produces child B, who would be ordered before child B. It would have been obvious for anyone to clearly see that mother A and her parents and grandparents are ordered before child B.

12. As per claim 10, Tudor does not specifically teach wherein incrementing the virtual clock associated with the first thread comprises incrementing the virtual clock associated with the first thread by one.

However, it would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to modify the teachings of Tudor with incrementing the virtual clock associated with the first thread comprises incrementing the virtual clock associated with the first thread by one in order to track forking and ordering.

13. As per claim 14, Tudor teaches if a thread accesses a shared memory location: updating the set of concurrent thread segments that access the location by forming a set comprising the union of (a) a set containing the current thread segment of the thread, and (b) a set containing the thread segments in the set of concurrent thread segments that continue to access the location; and if the updated set of concurrent thread segments contains at most one element, then updating the set of locks associated with the location to the set of locks associated with the thread, and otherwise: (i) updating the set of locks associated with the location to a set comprising the intersection of (a) the set of locks associated with the location and (b) the set of locks associated with the thread, and (ii) if the set of locks associated with the location is empty, reporting a warning of a potential race condition (Column 2, lines 33-52; Column 8, lines 35-60).

14. As per claim 15, Tudor does not specifically teach wherein the set containing the thread segments in the set of concurrent thread segments that continue to access the location is formed by computing a subset of the set of concurrent thread segments, wherein the subset contains each thread segment a that satisfies the following predicate: for every thread segment b in the set of thread segments ordered before a, at least one of the following is true: (i) the thread identifier of a is not equal to the thread identifier of b and (ii) the virtual clock value of a is greater than the virtual clock value of b.

However, it would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to modify the teachings of Tudor with wherein the set containing the thread segments in the set of concurrent thread segments that continue to access the location is formed by computing a subset of the set of concurrent thread segments, wherein the subset contains each thread segment a that satisfies the following predicate: for every thread segment b in the set of thread segments ordered before a, at least one of the following is true: (i) the thread identifier of a is not equal to the thread identifier of b and (ii) the virtual clock value of a is greater than the virtual clock value of b since this specific step allows one to further refine the set for more accurate race prediction.

15. Claims 16-19, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tudor, Patent No. 6,920634 (hereafter Tudor) in view of Hastings, Patent No. 5193180 (hereafter Hastings).

16. As per claims 16, 19, Tudor teaches a computer-implemented method for dynamic race detection by inserting additional instructions in the program, which can be done using techniques included in Hastings (Column 4, lines 61-67).

Tudor does not specifically teach that the compiler is inserting calls to the race detector in the compiled code and adding information required by the race detector to shared memory objects.

However, Hastings teaches a method of having a compiler that is capable of inserting extra instructions for the purpose of modifying code dynamically (Abstract; Column 13, lines 26-44).

It would have been obvious to one having ordinary skill in the art to combine the teachings of Tudor with implementing a compiler of a runtime system that inserts calls, as taught by Hastings, so that the compiler may call the race detector as disclosed by Tudor, because it allows for modifying the code dynamically. Moreover, since additional code is added using the method steps of Hastings, it is inherent that additional instructions of the race detector takes up memory space, and therefore, it is inherent that shared memory objects instrumentation information is added.

17. As per claims 17, Hastings teaches wherein inserting the calls to the race detector is by way of modifying the compiler of the runtime system (Column 13, lines 26-44).

18. As per claim 18, Tudor does not specifically teach wherein the memory allocator is an alteration of another memory allocator.

However, it would have been obvious to one having ordinary skill in the art to have the memory allocator contain any types of characteristic, including having it be an

alteration of another memory allocator since this characteristic does not contribute to the importance this the applicant's invention.

19. As per claim 21, Tudor teaches wherein adding the instrumentation information required by the race detector is by way of changing the memory allocator of the runtime system (Column 5, lines 12-22; Column 6, lines 52-61).

20. Claim 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tudor, Patent No. 6,920634 (hereafter Tudor) in view of A Comparative Analysis of Fine-Grain Threads Packages, Lowenthal et al., 2001 (hereafter Lowenthal) further in view of Hastings, Patent No. 5193180 (hereafter Hastings).

21. As per claim 22, it is a combination of claims 1 and 16, since claims 1 and 16 are both rejected as above, claim 22 is rejected as well.

Response to Arguments

22. Applicant's argument filed on 4/11/2008 regarding claims 1-22 have been fully considered but are not persuasive.

23. In the remark applicant argued in substance that:

i) Pg 10, Hastings teaches away from modifying the compiler.

ii) Pg 11, Tudor has no mentioning of any of the claim languages found in claim 21.

iii) Pg 9, it is clear from Para 12, 45, 46 what shared memory objects instrumentation information is.

24. The Examiner respectfully disagree with the applicant, as to point:

i) Even though Hastings does admit that modifying the compiler is difficult, he nonetheless includes this option in his alternative embodiment where he discloses that compiler may add extra code (Column 13, lines 27-35).

ii) Because claim 21 is vaguely stated, it is uncertain what the instrumentation information is and how the memory allocator relates to the added information, therefore the Examiner has interpreted this claim to broadly mean that additional objects are added. Since Tudor in view of Hastings teaches additional instructions are added to call and run the race detector, it is inherent that additional memory needs to be allocated to these additional instructions, therefore the memory allocator would need to change in such a way to accommodate the addition.

iii) These 3 paragraphs do not give a clear precise definition. It's meaning and purpose remains vague and unclear, therefore the Examiner has interpreted the term as broadly as possible.

Conclusion

25. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MENGYAO ZHE whose telephone number is (571)272-6946. The examiner can normally be reached on Monday Through Friday, 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195